CLAIM AMENDMENTS:

A listing of the entire set of pending claims 1-43 is submitted herewith per 37 C.F.R. §1 121. No new matter has been added with the amendments to claims 1, 11, 21, 26, 36, 39, 41 and 42. This listing of pending claims 1-43 will replace all prior versions, and listings, of claims in the application.

1. (Currently amended) A method for transitioning a debugging unit between a plurality of operating states, comprising:

defining a first set of operating instructions to be processed by a processor core;

defining a first triggering instruction to provide a first signal to the debugging unit whereby the debugging unit is operable to transition from a first debugging operating state to a second debugging operating state; and

embedding said first triggering instruction within said first set of operating instructions.

2. (Currently Amended) The method of claim 1, further comprising

coding said first set of operating instructions within a computer readable medium, said coded first set of operating instructions including a coded first triggering instruction;

operating said computer readable medium to provide an instruction stream to a processor core, said instruction stream representative of said coded first set of operating instructions, said instruction stream including a second signal representative of said coded first triggering instruction; and

operating said processor core to provide said first signal to the debugging unit in response to said second signal to thereby transition the debugging unit from the first debugging operating state to the second debugging operating state.

3. (Currently Amended) The method of claim 1, further comprising:

defining a second triggering instruction to provide a second signal to the debugging unit whereby the debugging unit is operable to transition from the second debugging operating state to the first debugging operating state; and

embedding said second triggering instruction within said first set of operating instructions.

4. (Currently Amended) The method of claim 3, further comprising:

coding said first set of operating instructions within a computer readable medium, said coded first set of operating instructions including a coded first triggering instruction and a coded second triggering instruction;

operating said computer readable medium to provide an instruction stream to a processor core, said instruction stream representative of said coded first set of operating instructions, said instruction stream including a third signal representative of said coded first triggering instruction and a fourth signal representative of said coded second triggering instruction;

operating said processor core to provide said first signal to the debugging unit in response to said third signal to thereby transition the debugging unit from the first operating debugging state to the second operating debugging state; and

subsequent to providing said first signal to the debugging unit, operating said processor core to provide said second signal to the debugging unit in response to said fourth signal to thereby transition the debugging unit from the second debugging operating state to the first debugging operating state.

5. (Currently Amended) The method of claim 1, further comprising:

defining a second triggering instruction to provide a second signal to the debugging unit whereby the debugging unit is operable to transition from the second debugging operating state to a third debugging operating state; and

embedding said second triggering instruction within said first set of operating instructions.

6. (Currently Amended) The method of claim 5, further comprising:

coding said first set of operating instructions within a computer readable medium, said coded first set of operating instructions including a coded first triggering instruction and a coded second triggering instruction;

operating said computer readable medium to provide an instruction stream to a processor core, said instruction stream representative of said coded first set of operating instructions, said instruction stream including a third signal representative of said coded first triggering instruction and a fourth signal representative of said coded second triggering instruction;

operating said processor core to provide said first signal to the debugging unit in response to said third signal to thereby transition the debugging unit from the first debugging operating state to the second debugging operating state; and

subsequent to providing said first signal to the debugging unit, operating said processor core to provide said second signal to the debugging unit in response to said fourth signal to thereby transition the debugging unit from the second debugging operating state to the third debugging operating state.

7. (Original) The method of claim 1, further comprising:

defining a second set of operating instructions to generate a first data or a second data; and

embedding said second set of operating instructions within said first set of operating instructions.

8. (Currently Amended) The method of claim 7, further comprising:

coding said first set of operating instructions within a computer readable medium, said first set of operating instructions including a coded first triggering instruction and a coded second set of operating instructions;

operating said computer readable medium to provide an instruction stream to a processor core, said instruction stream representative of said coded first set of operating instructions, said instruction stream including a second signal representative of said coded first triggering instruction and a set of signals representative of said coded second set of operating instructions;

operating said processor core to generate said first data or said second data in response to said set of signals; and

subsequent to a generation of said first data by said processor core, operating said processor core to provide said first signal to the debugging unit in response to said second signal to thereby transition the debugging unit from the first debugging operating state to the second debugging operating state.

9. (Currently Amended) The method of claim 1, further comprising:

further defining said first triggering instruction to provide a second signal to the debugging unit whereby the debugging unit is operable to transition from the first debugging operating state to a third debugging operating state;

defining a second set of operating instructions to generate either a first data or a second data; and

embedding said second set of operating instructions within said first set of operating instructions.

10. (Currently Amended) The method of claim 9, further comprising:

coding said first set of operating instructions within a computer readable medium, said first set of operating instructions including a coded first triggering instruction, and a coded second set of operating instructions;

operating said computer readable medium to provide an instruction stream to a processor core, said instruction stream representative of said coded first set of operating instructions, said instruction stream including a third signal representative of said coded first triggering instruction, and a set of signals representative of said coded second set of operating instructions;

operating said processor core to generate either said first data or said second data in response to said set of signals;

subsequent to a generation of said first data by said processor core, operating said processor core to provide said first signal to the debugging unit in response to said third signal to thereby transition the debugging unit from the first debugging operating state to the second debugging operating state; and

subsequent to a generation of said second data by said processor core, operating said processor core to provide said second signal to the debugging unit in response to said third signal to thereby transition the debugging unit from the first debugging operating state to the third debugging operating state.

11 (Currently Amended) A microprocessor, comprising:

a debugging unit operable to transition from a first debugging operating state to a second debugging operating state in response to a first signal; and

a processor core operable to fetch an instruction stream including a second signal representative of a first triggering instruction to transition said debugging unit from said first debugging operating state to said second debugging operating state, said processor core further operable to provide said first signal to said debugging unit in response to said second signal.

12. (Original) The microprocessor of claim 11,

wherein said processor core includes a register operable to provide said first signal to said debugging unit in response to a third signal including an address of said register.

13. (Currently Amended) The microprocessor of claim 11, wherein

said debugging unit is further operable to transition from said second debugging operating state to said debugging first operating state in response to a third signal;

said instruction stream further includes a fourth signal representative of a second triggering instruction to transition said debugging unit from said second debugging operating state to said first debugging operating state; and

said processor core is further operable to provide said third signal to said debugging unit in response to said fourth signal.

14. (Original) The microprocessor of claim 13, wherein said processor core includes

a first register operable to provide said first signal to said debugging unit in response to a fifth signal including an address of said first register; and

a second register operable to provide said third signal to said debugging unit in response to a sixth signal including an address of said second register.

15. (Currently Amended) The microprocessor of claim 11, wherein

said debugging unit is further operable to transition from said second debugging operating state to a third debugging operating state in response to a third signal;

said instruction stream further includes a fourth signal representative of a second triggering instruction to transition said debugging unit from said second debugging operating state to said third debugging operating state; and

said processor core is further operable to provide said third signal to said debugging unit in response to said fourth signal.

16. (Original) The microprocessor of claim 15, wherein said processor core includes

a first register operable to provide said first signal to said debugging unit in response to a fifth signal including an address of said first register; and

a second register operable to provide said third signal to said debugging unit in response to a sixth signal including an address of said second register.

17. (Original) The microprocessor of claim 11, wherein

said instruction stream further includes a set of signals representative of a set of operating instructions to operate said processor core to generate a first data or a second data;

said processor core is further operable to generate said first data or said second data in response to said set of signals; and

subsequent to a generation of said trigger data, said processor core is further operable to provide said first signal to said debugging unit in response to said second signal.

18. (Original) The microprocessor of claim 17,

wherein said processor core includes a register operable to provide said second signal to said debugging unit in response to a third signal including an address of said register and a fourth signal including said first data.

19. (Currently Amended) The microprocessor of claim 11, wherein

said debugging unit is further operable to transition from said first debugging operating state to a third debugging operating state in response to a third signal;

said first trigger instruction is to selectively transition said debugging unit from said first operating state to said second operating state or to transition said debugging unit from said first operating state to said third operating state;

said instruction stream further includes a set of signals representative of a set of operating instructions to operate said processor core to generate a first data or a second data;

said processor core is further operable to selectively generate said first trigger data or said second trigger data in response to said set of signals;

subsequent to a generation of said first data, said processor core is further operable to provide said first signal to said debugging unit in response to said second signal; and

subsequent to a generation of said second data, said processor core is operable to provide said third signal to said debugging unit in response to said second signal.

20. (Original) The microprocessor of claim 19,

wherein said processor core includes a register operable to provide said first signal to said debugging unit in response to a fourth signal including an address of said register and a fifth signal including said first data, and operable to provide said third signal to said debugging unit in response to a sixth signal including an address of said register and a seventh signal including said second data.

21. (Currently Amended) A computer readable medium storing a program for transitioning a debugging unit between a plurality of operating states, comprising:

a first computer readable code to operate a processor core; and

a second computer readable code to transition the debugging unit from a first debugging operating state to a second debugging operating state, said second computer readable code embedded within said first computer readable code.

22. (Currently Amended) The computer readable medium of claim 21, further comprising:

a third computer readable code to transition the debugging unit from said second debugging operating state to said first debugging operating state, said third computer readable code embedded within said first computer readable code.

23. (Currently amended) The computer readable medium of claim 21, further comprising:

a third computer readable code to transition the debugging unit from said second debugging operating state to a third debugging operating state, said third computer readable code embedded within said first computer readable code.

24. (Currently Amended) The computer readable medium of claim 21, further comprising:

a third computer readable code to operate said processor core to generate a first data or a second data, said third computer readable code embedded within said first computer readable code,

wherein said second computer readable code is to transition the debugging unit from said first debugging operating state to said second debugging operating state in response to a generation of said first data.

25. (Currently Amended) The computer readable medium of claim 21, further comprising:

a third computer readable code to operate said processor core to generate a first data or a second data, said third computer readable code embedded within said first computer readable code,

wherein said second computer readable code is to transition the debugging unit from said first debugging operating state to said second debugging operating state in response to a generation of said first data, and

wherein said second computer readable code is to transition the debugging unit from said first debugging operating state to a third debugging operating state in response to a generation of said second data.

26. (Currently Amended) A system for transitioning a debugging unit between a plurality of operating states, comprising:

a computer readable medium including a first computer readable code to transition the debugging unit from a first debugging operating state to a second debugging operating state, said computer readable medium operable to provide a first signal representative of said first computer readable code; and

a processor core operable to provide a second signal to the debugging unit in response to said first signal whereby the debugging unit is operable to transition from the first debugging operating state to the second debugging operating state.

27. (Original) The system of claim 26,

wherein said processor core includes a register operable to provide said second signal in response to a third signal including an address of said register.

28. (Currently Amended) The system of claim 27, wherein

said computer readable medium further includes a second computer readable code to transition the debugging unit from the second debugging operating state to the first debugging operating state, said computer readable medium operable to provide a third signal representative of said second computer readable code; and

said processor core is further operable to provide a fourth signal to the debugging unit in response to said third signal whereby the debugging unit is operable to transition from the second debugging operating state to the first debugging operating state.

29. (Original) The system of claim 28, wherein said processor core includes

a first register operable to provide said second signal to the debugging unit in response to a fifth signal including an address of said first register; and

a second register operable to provide said fourth signal to the debugging unit in response to a sixth signal including an address of said second register.

30. (Currently Amended) The system of claim 27, wherein

said computer readable medium further includes a second computer readable code to transition the debugging unit from the second debugging operating state to a third debugging operating state, said computer readable medium operable to provide a third signal representative of said second computer readable code; and

said processor core is further operable to provide a fourth signal to the debugging unit in response to said third signal whereby the debugging unit is operable to transition from the second debugging operating state to the third debugging operating state.

31. (Original) The system of claim 30, wherein said processor core includes

a first register operable to provide said second signal to the debugging unit in response to a fifth signal including an address of said first register; and

a second register operable to provide said fourth signal to the debugging unit in response to a sixth signal including an address of said second register.

32. (Original) The system of claim 27, wherein

said computer readable medium further includes a second computer readable code to operate said processor core to generate a first trigger data or a second trigger data, said computer readable medium operable to provide a set of signals representative of said second computer readable code;

said processor core is further operable to selectively generate said trigger data in response to said set of signals; and

subsequent to a generation of said first data, said processor core is operable to provide said first signal to the debugging unit in response to said second signal.

33. (Original) The system of claim 32,

wherein said processor core includes a register operable to provide said second signal to the debugging unit in response to a third signal including an address of said register and a fourth signal including said trigger data.

34. (Currently Amended) The system of claim 27, wherein

said first computer readable code is to selectively transition the debugging unit from the first debugging operating state to the second debugging operating state or from the first debugging operating [[sate]] state to a third debugging operating state;

said computer readable medium further includes a second computer readable code to operate said processor core to generate a first data or a second data, said computer readable medium operable to provide a set of signals representative of said second computer readable code;

said processor core is further operable to selectively generate said first data or said trigger data in response to said set of signals;

subsequent to a generation of said first data, said processor core is operable to provide said second signal to the debugging unit in response to said first signal; and

subsequent to a generation of said second data, said processor core is operable to provide a fourth signal to the debugging unit in response to said first signal whereby the debugging unit is operable to transition from the first debugging operating state to the third debugging operating state.

35. (Original) The system of claim 34,

wherein said processor core includes a register operable to provide said second signal to the debugging unit in response to a fourth signal including an address of said register and a fifth signal including said first data, and to provide said third signal to the debugging unit in response to a sixth signal including said address of said register and a seventh signal including said second data.

36. (Currently Amended) A method for transitioning a debugging unit between a plurality of operating states, comprising:

receiving a first signal representative of a first triggering instruction to transition the debugging unit from a first debugging operating state to a second debugging operating state; and

processing said first signal to thereby transition the debugging unit from said first debugging operating state to said second debugging operating state.

37. (Currently Amended) The method of claim 36,

receiving a second signal representative of a second triggering instruction to transition the debugging unit from said second debugging operating state to said first debugging operating state; and

processing said second signal to thereby transition the debugging unit from said second debugging operating state to said first debugging operating state.

38. (Currently Amended) The method of claim 36,

receiving a second signal representative of a second triggering instruction to transition the debugging unit from said second debugging operating state to a third debugging operating state; and

processing said second signal to thereby transition the debugging unit from said second debugging operating state to said third debugging operating state.

39 (Currently Amended) A method for transitioning a debugging unit between a plurality of operating states, comprising:

receiving a set of operating signals representative of a set of operating instructions to generate a first data or a second data;

receiving a trigger instruction signal representative of a triggering instruction to transition the debugging unit from a first debugging operating state to a second debugging operating state in response to a generation of said first data; and

processing said set of operating signals and said trigger instruction signal to thereby transition the debugging unit from said first debugging operating state to said second debugging operating state in response to a generation of said first data.

40. (Original) A method for transitioning a debugging unit between a plurality of operating states, comprising:

receiving a set of operating signals representative of a set of operating instructions to generate a first data or a second data;

receiving a trigger instruction signal representative of a triggering instruction to transition the debugging unit from a first operating state to a second operating state in response to a generation of said first data and to transition the debugging unit from said first operating state to a third operating state in response to a generation of said second data; and

processing said set of operating signals and said trigger instruction signal to thereby transition the debugging unit from said first operating state to said second operating state in response to a generation of said first data and to thereby transition the debugging unit from said first operating state to said third operating state in response to a generation of said second data.

41. (Currently Amended) A method, comprising:

providing a computer readable medium operable to provide a first signal representative of a first triggering instruction to transition a debugging unit from a first debugging operating state to a second debugging operating state;

providing a processor core operable to provide a second signal in response to said first signal; and

providing a debugging unit operable to transition from said first debugging operating state to said second debugging operating state in response to said second signal.

42. (Currently Amended) A method, comprising:

providing a computer readable medium operable to provide a set of operating signals representative of a set of operating instructions to generate a first data or a second data, and a trigger instruction signal representative of a triggering instruction to transition a debugging unit from a first debugging operating state to a second debugging operating state;

providing a processor core operable to generate said first data or said second data in response to said set of operating signals, and to provide a triggering signal subsequent to a generation of said first data in response to said trigger instruction signal; and

providing a debugging unit operable to transition from said first debugging operating state to said second debugging operating state in response to said triggering signal.

43. (Previously presented) A method, comprising:

providing a computer readable medium operable to provide a set of operating signals representative of a set of operating instructions to generate a first data or a second data, and a trigger instruction signal representative of a triggering instruction to transition said debugging unit from a first operating state to a second operating state or to transition said debugging unit from said first operating state to a third operating state;

providing a processor core operable to generate said first data or said trigger data in response to said set of operating signal, to provide a first triggering signal subsequent to a generation of said first data in response to said triggering instruction signal, and to provide a second triggering signal subsequent to a generation of said second data in response to said triggering instruction signal; and

providing a debugging unit operable to transition from said first operating state to said second operating state in response to said first triggering signal and to transition from said first operating state to said third operating state in response to said second triggering signal.